EE 330 Fall 2024 HW4 Solutions

1) No of wafers produced by 248nm in 4 years= 80x24x365x4 = 2803200
   cost per wafer for 248nm machine = 10M/2803200 =$3.17
   cost per process = $35.7.

   No of wafers produced by 193nm in 4 years= 20x24x365x4 = 700800
   cost per wafer for 248nm machine = 40M/700800 =$57.08

   cost per process = $570.8

   wafer area = pi*(300*10^{-3})^2/4 = 70650 sq mm

   die area of 90nm chip is 50 sq mm.

   die/wafer for 90nm wafer = wafer area/die area = 1413 dies/ wafer

   die area of 50nm chip is going to reduce by a factor of (90/50)^2

   This gives us the die area of the 50nm chip = 15.43 mm^2

   die/wafer for 50nm wafer = wafer area/die area = 4578 dies /wafer

   cost per chip of a 248nm machine = 35.7/1413 = $0.025 per chip

   cost per chip of a 193nm = 570.8/4578 = $ 0.125 per chip

   Therefore, we can say that it costs about 5 times more to manufacture a chip at 50nm node.

2) Gate oxide thickness of Si-O2 = 2nm

$$\frac{\varepsilon(SiO2) * A}{d_{SiO2}} = \frac{\varepsilon(HfO2) * A}{d_{HfO2}}$$

   We take the $\varepsilon(SiO2) = 3.9$ and $\varepsilon(HfO2) = 20$

   We get the gate oxide thickness of HfO2 = 10.3nm

3) From lecture notes, diameter of oxide layer = 0.35nm

→ Volume of oxide layer = $\frac{4}{3}\pi\left(0.\frac{35}{2}\right)^3 = 0.0224493\,nm^3$

→ Volume of oxide layer = $7nm \times 14nm \times 25\times10^{-10}\,m$

$= 245\,nm^3$

⇒ Number of Silicon dioxide molecules = $\frac{245\,nm^3}{0.0224493\,nm^3}$

$= 10913.5$ molecules

4) The resistivity of Al = $2.65 * 10^{-8}\,\Omega\cdot m$

Resistance = $\rho\frac{L}{A}$

$= 2.65\times10^{-8} \times \frac{1000\times10^{-6}}{20\times10^{-9}\times 40\times10^{-9}}$

$= 33125\,\Omega$

5) The lowest resistance material would be Silver. One of the reasons is that they are not used to form metal connects because they are more immune to oxidization as compared to Cu or Al . Also, during the metallization process, they can migrate and enter the Silicon which alters the behavior of the CMOS.

6) The loss of material per cut = 150um
Typical thickness of 12” silicon wafer = 775um.
Thickness of material removed from Silicon pull per wafer = 150um + 775um = 925um
Total number of wafers from the Silicon pull = 2/925u = 2126 wafers
There is an additional 0.162*925u = 149.85um of Silicon being wasted in the process.

7)

Contact resistance → 14.6 ohms

poly sheet → 21.7 ohms/sq

Capacitance poly → $82\ aF/\mu m^2 = 82 \times 10^{-18}\ F/um^2$

(a) $1K\ Hz = \frac{1}{RC}$, Capacitance = $8_p\ F$

Capacitor Area

8_pF = Capacitance poly x Capacitor Area

$\Rightarrow$ Capacitor Area = $\frac{8_pF}{\text{Capacitance poly}} = \frac{8 \times 10^{-12}\ F}{82 \times 10^{-18}\ F/um^2}$

$\Rightarrow$ Capacitance Area = $97560.98\ \mu m^2$

Resistor Area

$$1000 \times 2\pi = \frac{1}{8_pF \times ((14.6 \times 2) + (21.7 \times N_s))}$$

$\rightarrow$ $N_s = 916790 =$ $\frac{\text{Resistor length}}{\text{Resistor width}}$

If Resistor length = 1 um

Resistor width = 916790 um

$\Rightarrow$ Resistor Area = $916790\ um^2$

$\rightarrow$ Total Filter Area = $916790\ um^2 + 97560.98\ um^2$

$= 1014350.98\ \mu m^2$

$\rightarrow$ Capacitor = 8pF

Resistor = $\frac{1}{2\pi \times 1000 \times 8p} = 19.894368\ M\Omega$

(b) Area of Capacitor + Area of resistor = Total Area

$\rightarrow A_{capacitor} + A_{resistor} = A_{total}$

$$(2\pi \times 1000) = \frac{1}{(82 \times 10^{-18} \times A_{cap}) \times [(14.6 \times 2) + 21.7 \times N_S]}$$

$A_{resistor} = N_S \times$ dimension of square

$\rightarrow$ 0.6 µm is minimum for 0.5µ technology

thus, to find minimum area, dimension of square $= (0.6\mu m)^2$

$$\Rightarrow (2\pi \times 1000) = \frac{1}{(82 \times 10^{-18} \times A_{cap}) \times \left[(2 \times 14.6) + \left(21.7 \times \frac{A_{res}}{(0.6\mu m)^2}\right)\right]}$$

$$\Rightarrow 2000\pi = \frac{1}{(82 \times 10^{-18} \times A_{cap}) \times \left[(2 \times 14.6) + 21.7 \times \frac{A_{total} - A_{cap}}{0.36}\right]}$$

let $A_{cap} = x$

$$A_{total} = x - 4.84424 \times 10^{-13} + 3.21995 \times 10^{10}\, x^{-1}$$

→ Minimum $A_{total} = (A_{total})' = 0$

$$(A_{total})' = 1 - 3.21995 \times 10^{10} x^{-2}$$

$$\Rightarrow (A_{total})' = 1 - \frac{3.21995 \times 10^{10}}{(A_{cap})^2} = 0$$

$$\Rightarrow A_{cap} = \sqrt{3.21995 \times 10^{10}} = \underline{179442.2\ \mu m^2}$$

$$\Rightarrow A_{total} = 179442.2 - 4.84424 \times 10^{-13} + \frac{3.21995 \times 10^{10}}{179442.2}$$

$$= \underline{358884.4\ \mu m^2}$$

$$\Rightarrow A_{resistor} = 358884.4 - 179442.2 = \underline{179437.4\ \mu m^2}$$

Comparing the values obtained in part (b) to (a), it can be observed that the values obtained in part (a) are 3 times higher than (b)

8) A) width and length dimensions are overlap of polysilicon gate and active area
width = 3µm
length = 1µm

B) Positive photoresist = exposed material is removed when developed
W is not affected by the dimensions of the Poly, only by dimensions of active but L is affected
Underdeveloped photoresist = not enough is removed,
Under-etched = not enough is removed . It follows if L1 is the original length (1u),

L=L1-2*0.1-2*0.1 = 0.6u and W = 3u

C) Negative photoresist = unexposed material is removed when developed
As before, W is not affected by the dimensions of Poly but L is affected

Underdeveloped photoresist = too little is removed but since negative photoresist, provides too much polysilicon protection . Under-etched, not enough is removed.

Thus L = L1 +2*(0.1) -2*(0.1) = 1u+0.2u – 0.2u =1u and W=3u

Note in this case the two deviations compensate for each other and the desired length is obtained.

9)

(i) $R = \rho \frac{L}{A} = \rho \frac{L}{\text{width} \times \text{thickness}}$

$\Rightarrow \text{thickness} = \frac{L \rho}{R \times \text{width}}$

Resistivity of aluminium $= 2.65 \times 10^{-8}\ \Omega\text{-m}$

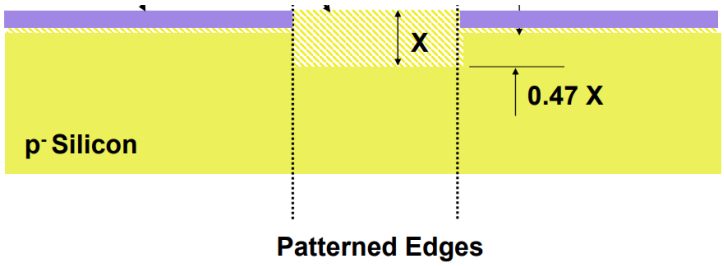
$\Rightarrow \text{thickness} = \frac{250 \times 10^{-6} \times 2.65 \times 10^{-8}}{25 \times 2 \times 10^{-6}} = 1.325 \times 10^{-7}\ \text{m}$

(ii) Resistivity of Copper $= 1.72 \times 10^{-8}\ \Omega\text{-m}$

$\Rightarrow 25\ \Omega = 1.72 \times 10^{-8} \times \frac{L}{1.325 \times 10^{-7} \times 2 \times 10^{-6}}$

$\Rightarrow L = 3.852 \times 10^{-4}\ \text{m}$

10)



Patterned Edges

Difference in wafer thickness $= 5000 \times 10^{-10} \times (1 - 0.47)$

$= 2.65 \times 10^{-7}$ m